

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the Application of:

Ramanujan Valmiki, et al.

U.S. Serial No.: 10/666,702

Filed: September 19, 2003

For: VIDEO AND GRAPHICS SYSTEM
WITH MPEG SPECIFIC DATA
TRANSFER COMMANDS

Examiner: Dastouri, Mehrdad

Group Art Unit: 2621

Confirmation No.: 1993

ELECTRONICALLY FILED
On March 30, 2007

**LITIGATION STATEMENT PURSUANT TO MPEP § 2001.06(C) and INFORMATION
DISCLOSURE STATEMENT**

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The owner of record of the present application, Broadcom Corporation, is currently involved in a patent infringement action with Qualcomm, Inc., Case No. 06-CV-0660 B, pending in the Southern District of California.

Pursuant to MPEP 2001.06(c), the Applicants would like to bring to the attention of the U.S. Patent and Trademark Office that the subject matter currently being claimed in the present application may be related to at least one of the patents currently asserted by Broadcom in the above-mentioned lawsuit.

The Applicants have also attached with this electronic submission a completed PTO form PTO/SB/08A which has seven (7) pages. Copies of each printed reference listed in the PTO/SB/08A form are attached with this electronic submission. Applicants, however, have not

Patents or other references previously provided to or by the PTO in this application. Fifty-seven (57) references are attached in this electronic submission.

The references being submitted have been either cited, produced or relied upon by Qualcomm thus far during the above-mentioned lawsuit. This submission is in no way intended as an admission that the submitted references constitute prior art under any subsection of 35 U.S.C. §102 or §103. Applicant expressly retains the right to argue that any of the cited references are not indeed prior art or to take any actions necessary to remove any of the cited references from the available prior art.

The Examiner is requested to initial the attached PTO/SB/08A and return one copy to the applicants to indicate consideration of the attached references.


A fee in the amount of \$180 is believed to be due because:

- * The applicant(s) believe(s) that this statement and enclosures are being filed after the first Office action on the merits has been mailed by the PTO. The basis of this belief is that an Office action on the merits appears to have been received by the undersigned to date.

The Commissioner is hereby authorized to charge any fees which are presently required, or credit any overpayment, to Deposit Account No. 13-0017.

Respectfully submitted,

Date: March 30, 2007



Mirut P. Dalal
Reg. No. 44,502
McAndrews, Held & Malloy, Ltd.
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Chicago, Illinois 60661
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet 1 of 7

Complete if Known

Application Number	10/666,702
Filing Date	September 19, 2003
First Named Inventor	Ramanujan Valmiki
Group Art Unit	2621
Examiner Name	Dastouri, Mehrdad
Attorney Docket Number	17440US02

U.S. PATENT DOCUMENTS

Examiner Initial*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	A1	4,020,332	04-26-1977	Crochiere et al.	
	A2	4,367,466	01-04-1983	Takeda et al.	
	A3	4,532,547	07-30-1985	Bennett	
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	A6	4,954,970	09-04-1990	Walker et al.	
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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450 Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. Send TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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Sheet 2 Of 7

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		Number-Kind Code ² (if known)			
	A38	5,621,869	04-15-1997	Drews	
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Group Art Unit	2621
Examiner Name	Dastouri, Mehrdad
Attorney Docket Number	17440US02

Sheet	3	Of	7
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	A122	6,133,901	10-17-2000	Law	
	A123	6,151,030	11-21-2000	DeLeeuw et al.	
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FOREIGN PATENT DOCUMENTS						
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	B1	EP 0746116 A2	12-04-1996	Hiratsuka		
	B2	EP 0 752 695	01-08-1997	O'Sullivan		
	B3	EP 0840276 A2	05-06-1998	Benbassat		
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	B6	GB 2287627 A	03-01-1995	Wong		
	B7	WO 94/10641	05-11-1994	Mical		
	B8	WO 00/28518	05-18-2000	MacInnis		

OTHER ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
	C1	Plaintiff and Counterdefendant Qualcomm Incorporated's Preliminary Invalidity Contentions For U.S. Patent 6,501,480 and 6,570,579
	C2	Thomas Porter & Tom Duff, "Compositing Digital Images", Computer Graphics, Vol. 18, No. 3, July 1984, pp. 253-259
	C3	Akeley, K. & Jermoluk T., "High-Performance Polygon Rendering," 22 Computer Graphics No. 4 (ACM August 1988).
	C4	Apgar, B., et al., "A Display System for the Stellar Graphics Superconductor Model GS1000," 22 Computer Graphics No. 4 (ACM August 1988).
	C5	Asal, M.D., et al., "Novel Architecture for a High Performance Full Custom Graphics Processor," (IEEE 1989).
	C6	Awaga, M., et al., "3D Graphics Processor Chip Set," (IEEE December 1995).
	C7	Cox, M. & Bhandari, N., "Architectural Implications of Hardware-Accelerated Bucket Rendering on the PC," (Association for Computing Machinery SIGGRAPH/Eurographics Workshop 1997).
	C8	Cyrix Corporation Manual, copyrighted 1996, 1997, and all underlying development work.
	C9	Deering, M., et al., "The Triangle Processor and Normal Vector Shader: A VLSI System for High Performance Graphics," 22 Computer Graphics No. 4 (ACM August 1988).
	C10	Donovan, W., et al., "Pixel Processing in a Memory Controller," (IEEE Computer Graphics and Applications 1995).
	C11	Dutton, T., "The Design of the DEC 3000 Model 500 AXP Workstation," (IEEE 1993).
	C12	Foley, James, D., et al., "Introduction to Computer Graphics," (Addison-Wesley Publishing Co. 1994) ("Introduction to Computer Graphics").
	C13	Galbi, D., et al., "An MPEG-1 Audio/Video Decoder with Run-Length Compressed Antialiased Video Overlays," (1995 IEEE International Solid-State Circuits Conference).
	C14	Glaskowsky, Peter, "Cyrix Creates Ultimate CPU for Games," Microprocessor Report, December 8, 1997.
	C15	Glaskowsky, Peter, "Intel Displays 740 Graphics Chip: Auburn Sets New Standard for Quality - But Not Speed," Microprocessor Report No. 2, February 16, 1998.
	C16	Gwennap, L., "Verite: A Programmable 3D Chip: Rendition Uses Internal RISC CPU for Versatility, Performance," 10 Microprocessor Report No. 6, May 6, 1996.

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Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
	C17	Hosotani S., et al., "A Display Processor Conforming to all DTV Formats with 188-TAP FIR Filters and 284 Kb FIFO Memories," (IEEE 1997 (Manuscript received June 13, 1997)).
	C18	Knittel, G. & Straber, W., "VIZARD - Visualization Accelerator for Realtime Display," (Association for Computing Machinery SIGGRAPH/Eurographics Workshop 1997).
	C19	Lewis, R., et al., "Delivering PCI in HP B-Class and C-Class Workstations: A Case Study in the Challenges of Interfacing with Industry Standards," (Hewlett-Packard Journal May 1998).
	C20	Manepally, R. & Sprague, D., "Intel's i750 (R) Video Processor -- The Programmable Solution," (IEEE 1991).
	C21	McCormack, J., et al., "Neon: A Single-Chip 3D Workstation Graphics Accelerator," (SIGGRAPH Eurograph Workshop Graph Hardware August 31, - Sept. 1, 1998).
	C22	Norrod, F. & Wawrzynak, R., "A Multimedia-Enhanced x86 Processor, Digest of Technical Papers," ISSCC96 (February 9, 1996).
	C23	Oguchi, T., et al., "A Single-Chip Graphic Display Controller," (1981 IEEE International Solid-State Circuits Conference).
	C24	Soferman, Z., et al., "Advanced Graphics Behind Medical Virtual Reality: Evolution of Algorithms, Hardware, and Software Interfaces," 86 Proceedings of the IEEE No. 3 (IEEE March 1998 (Manuscript received July 3, 1997)).
	C25	Scott, N., et al., "An Overview of the VISUALIZE fx Graphics Accelerator Hardware," (Hewlett-Packard Journal May 1998) and all underlying development work ("HP").
	C26	Sumi, M., et al., "A 40-Mpixel/s Bit Block Transfer Graphics Processor," (IEEE 1989).
	C27	Foley, James D., et al.; Computer Graphics: Principles and Practice; publication, 1996, 1990; The Systems Programming Series, 4 pages, Second Edition in C; Addison-Wesley Publishing Company, U.S.A.
	C28	Tobias, R., "The LR33020 GraphX Processor: A Single Chip X-Terminal Controller," (IEEE 1992).
	C29	Watkins, J., et al., "A Memory Controller with an Integrated Graphics Processor (IEEE 1993).
	C30	Yao, Yong, "Samsung Launches Media Processor: MSP Is Designed for Microsoft's New 3D-Software Architecture," 10 Microprocessor Report No. 11, August 26, 1996.
	C31	Yao, Yong, "Competition Heats Up in 3D Accelerators: Market Hungers for a Unified Multimedia Platform from Microsoft," 10 Microprocessor Report No. 15, November 18, 1996.
	C32	Yao, Yong, "Chromatic's Mpac2 Boosts 3D: Mpac/3000 Becomes First Media Processor to Ship in Volume," 10 Microprocessor Report No. 15, November 18, 1996.
	C33	Motorola, Inc. MC92100 "Scorpion" Graphics Display Generator, SDRAM Controller, and Digital Video Encoder, 1997, 6 pages.
	C34	Power TV, Inc., Eagle™ Graphics/Audio Media Compositor Data Sheet, Version 1.7, Feb. 27, 1997, pp. 63.
	C35	Berekovic, M. & Pirsch, P., "Architecture of a Coprocessor Module for Image Compositing," (IEEE 1998).
	C36	Blinn, J., "Compositing, Part I: Theory," (IEEE September 1994).
	C37	Blinn, Jim; Jim Blinn's Corner Dirty Pixels; publication; 1998; pp. 179-190; Chapter Sixteen; Morgan Kaufmann Publishers, Inc.; San Francisco, CA, U.S.A.
	C38	Jaspers, et al., "A Flexible Heterogeneous Video Processor System for Television Applications," (IEEE Sept. 25, 1998).
	C39	Li, R., et al., "A Flexible Display Module for DVD and Set-Top Box Applications," (IEEE Transactions on Consumer Electronics August 1997 (Manuscript received June 13, 1997)).

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Substitute for form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Complete if Known	
				Application Number	10/666,702
				Filing Date	September 19, 2003
				First Named Inventor	Ramanujan Valmiki
				Group Art Unit	2621
				Examiner Name	Dastouri, Mehrdad
				Attorney Docket Number	17440US02
Sheet	7	Of	7		

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	C40	Ostermann, J., "Coding of Arbitrarily Shaped Objects with Binary and Greyscale Alpha-Maps: What Can MPEG-4 Do for You?," (Proceedings of the 1998 IEEE International Symposium on Circuits and Systems, May 31-June 3, 1998, Vol. 5).
	C41	Stytz, et al., "Three-Dimensional Medical Imaging: Algorithms and Computer Systems," (ACM Computing Surveys, December 1991).
	C42	Wang, J. & Adelson, E., "Representing Moving Images with Layers," (IEEE Transactions on Image Processing, September 1994).
	C43	Sun, Huifang et al., "A New Approach for Memory Efficient ATV Decoding," 1997 IEEE International Conference on Consumer Electronics, pp. 174-175, Los Angeles, 1997.
	C44	Bao, Jay et al., "HDTV Down-Conversion Decoder," IEEE Transactions on Consumer Electronics, pp. 402-410, vol. 42, No. 3, Aug. 1996.
	C45	Mokry, Robert et al., "Minimal Error Drift in Frequency Scalability for Motion-Compensated DCT Coding," IEEE Transactions on Circuits and Systems for Video Technology, pp. 392-406, vol. 4, No. 4, Aug. 1994.
	C46	Vetro, Anthony et al., "Minium Drift Architectures for 3-Layer Scalable DTV Decoding," IEEE Transactions on Consumer Electronics, pp. 527-536, vol. 44, No. 3, Aug. 1998.
	C47	Lee, Dong-Ho et al., "HDTV Video Decoder Which Can Be Implemented With Low Complexity," IEEE International Conference on Consumer Electronics, pp. 6-7, 1994.
	C48	Sun, Huifang, "Hierarchical Decoder for MPEG Compressed Video Data," IEEE Transactions for Consumer Electronics, pp. 559-564, vol. 39, No. 3, Aug. 1993.
	C49	Yu, Haoping et al., "Block-Based Image Processor for Memory Efficient MPEG Video Decoding," 1999 IEEE International Conference on Consumer Electronics, pp. 114-115, 1999.

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